TFT MODULE SPECIFICATION

RVT43HLBNWCA0 V2.0A

EVE 4 IPS RGB 4.3” display datasheet
Rev. 1.0
2026-08-04

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ITEM	CONTENTS	UNIT
LCD Type	TFT/Transmissive/Normally black/IPS	/
Size	4.3	Inch
Viewing Direction	Free	/
Outside Dimensions (W x H x D)	105.50 x 67.20 x 10.57	mm
Active Area (W x H)	95.04 x 53.86	mm
Pixel Pitch (W x H)	0.198 x 0.198	mm
Resolution	480 x 272 (RGB)	/
Brightness	800	cd/m^2
Interface	SPI/QSPI	/
QSPI Flash Memory size	256	Mb
Host Connector	RiBUS, ZIF 20 pin, 0.5mm pitch, down-side contact	/
Color Depth	16.7 M	/
Pixel Arrangement	RGB Vertical Stripe	/
Driver IC of Board	BT817Q	/
With/Without Touch	With Capacitive Touch Panel	/
CTP IC	ILI2132A	/
LCD Input Voltage	3.3	V
Supply Voltage for Backlight	5.0 (TYP.)	V
Audio amplifier	Build in class-D 1.5W audio amplifier	/
Bonding Technology	Air Bonding	/
Weight	TBD	g

Note 1. RoHS3 compliant

Note 2. LCM weight tolerance: ± 5%.

1. REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
1.0	2026-08-04	Initial release	

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3. MODULE CLASSIFICATION INFORMATION

RV	T	43	H	L	T	N	W	C	A0	V2.0A
1.	2.	3.	4.	5.	6.	7.	8.	9.	10.	11.

NO.	PARAMETER	SYMBOL
1.	BRAND	RV – Riverdi
2.	PRODUCT TYPE	T – TFT Standard
3.	DISPLAY SIZE	43 – 4.3”
4.	MODEL SERIAL NO.	H – High Brightness, IPS
5.	RESOLUTION	L – 480 x 272 px
6.	INTERFACE	B – SPI/QSPI
7.	FRAME	N – Without Mounting Metal Frame
8.	BACKLIGHT TYPE	W – LED White
9.	TOUCH PANEL	C – With Capacitive Touch Panel
10.	VERSION	A0 – aTouch
11.	MODULE REVISION	V2.0A

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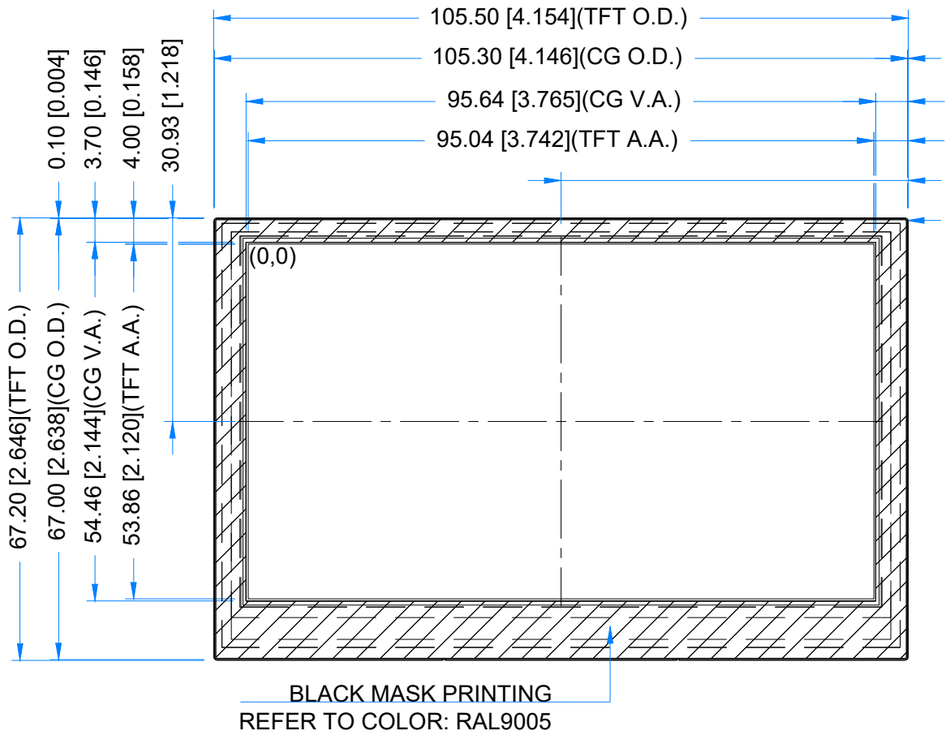
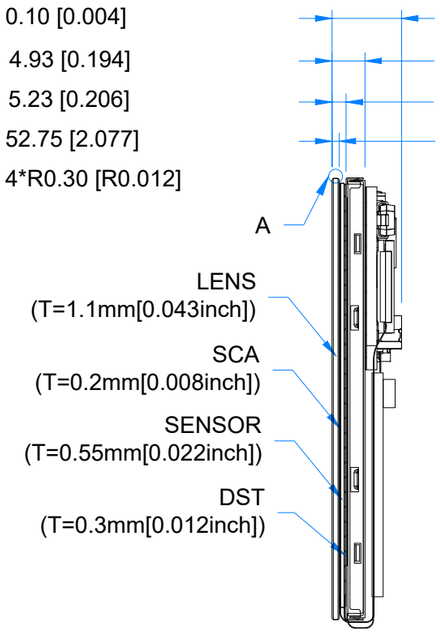
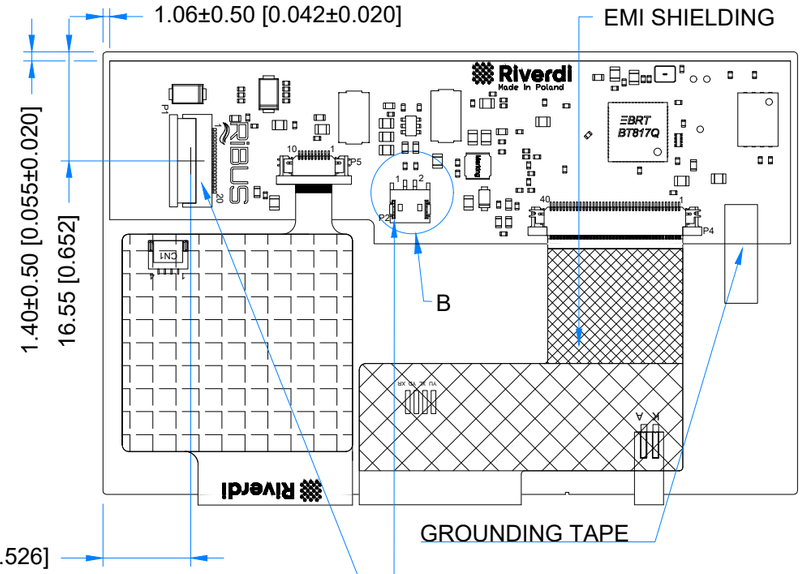
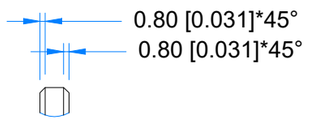
Revision:	Changes:	Date:
1.0	Initial Case	2026.02.10



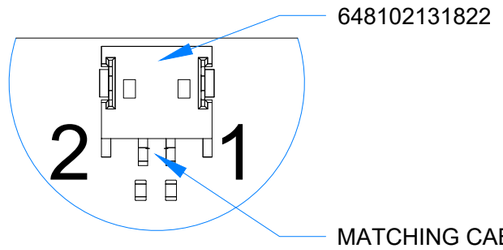


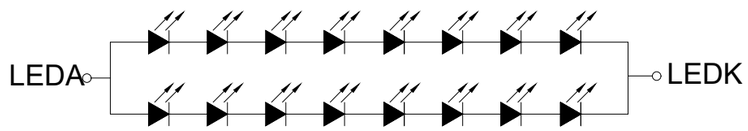


DETAIL A
SCALE 4:1



DETAIL B
SCALE 4:1





LED Diagram Circuit

TFT NOTES:
1. DISPLAY TYPE: TRANSMISSIVE, NORMALLY BLACK, IPS
2. RESOLUTION: 480x272
3. VIEWING ANGLE: FREE
4. INTERFACE: SPI/QSPI
5. DRIVER IC ON THE BOARD: BT817Q
6. SUPPLY VOLTAGE FOR MODULE: 3.3V
7. SUPPLY VOLTAGE FOR BACKLIGHT: 5.0V, BUIILT-IN LED DRIVER

TP NOTES:
1. TP STRUCTURE: G+G
2. CG THICKNESS: 1.1mm[0.043inch]
3. DRIVER IC: ILI2132A
4. SURFACE HARDNESS:7H
5. INTERFACE: SPI/QSPI VIA RIBUS AND BT817Q

GENERAL NOTES:
1. SURFACE LUMINANCE: 800cd/m^2
2. OPERATING TEMPERATURE: -20°C ~ 70°C
3. STORAGE TEMPERATURE: -30°C ~ 80°C
4. WITHOUT INDIVIDUAL TOLERANCE: ±0.3mm
5. RoHS COMPLIANT

PN: RVT43HLBNWCA0 V2.0A				Riverdi
SN:				
DRAWN:	M.Stabinski	2026.02.10	1:0.93	
CHECKED:	M.Wierzbowski	2026.02.10	[mm]	
APPR:	M.Wierzbowski	2026.02.10	ISO A3	P. 1 of 1

5. ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage for Module	VDD	0	3.6	V	Note 1
Digital I/O signals (SPI/QSPI/GPIO) Voltage	-	-0.5	3.3		Note 1, 2
Supply voltage for Backlight	BLVDD	-0.3	7.0		Note 1
Operating Temperature	T_{OP}	-20	70	°C	
Storage Temperature	T_{ST}	-30	80	°C	

Note 1. Exceeding maximum values may cause improper operation or permanent damage to the unit.

Note 2. Digital I/O signals are to be connected to pins 3 ÷ 9, 11 and 12 pins at RiBUS connector (P1).

6. ELECTRICAL CHARACTERISTICS

PARAMETER		SYMBOL	MIN	TYP	MAX	UNIT
Digital supply voltage		V_{DD}	3.0	3.3	3.6	V
Input Signal Voltage	Low Level	V_{IL}	0	-	0.8	V
	High Level	V_{IH}	2.0	-	5.5	V

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Current drawn from VDD@3.3V	I_{VDD}	-	190	260	mA	Note 1

Note 1. Animated pictures are displayed on the screen and there is no QSPI communication during the measurement of TYP and MAX values.

TYP value is measured when the audio is off.

MAX value is measured when the audio is on, and volume is set to maximum.

7. BACKLIGHT ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage for Backlight	BLVDD	4.5	5.0	5.5	V	Notes 1, 2
Backlight Lifetime	-	-	50,000	-	hours	Note 3

Note 1. Unless specified, the ambient temperature T_a = 25℃

Note 2. The recommended operating conditions refer to a range in which operation of this product is guaranteed. Should this range be exceeded, the operation cannot be guaranteed even if the values may be without the absolute maximum ratings.

Note 3. If LED is driven by high current, the lifetime of LED will be reduced. Operating life means brightness goes down to 50% initial brightness. Typical operating lifetime is estimated data.

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Current drawn from BLVDD @4.5V	I_{BLVDD}	4.90	125	310	mA	Note 3
Current drawn from BLVDD @5.0V		4.80	110	240	mA	
Current drawn from BLVDD @5.5V		5	100	170	mA	

Note 3. To control the backlight dimming, please refer to subchapter 11.4.

MIN BL is when REG_PWM_DUTY = 1

50% BL is when REG_PWM_DUTY = 64

100% BL is when REG_PWM_DUTY = 128

8. ELECTRO-OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	RMK	NOTE
Response Time	Tr+Tf	θ=0° ø=0° Ta=25 °C	-	30	40	ms	FIG 1.	4, 7
Contrast Ratio	Cr		640	800	-	---	FIG 2.	1, 7
Surface Luminance	Lv		-	800	-	cd/m 2		2, 7
Uniformity	U	-	75	80	-	%	FIG 2.	3
Viewing Angle Range	θ	ø = 90°	70	80	-	deg	FIG 3.	6
		ø = 270°	70	80	-	deg		
		ø = 0°	70	80	-	deg		
		ø = 180°	70	80	-	deg		
CIE (x, y) Chromaticity	Rx	θ=0° ø=0° Ta=25 °C	0.560	0.590	0.620	-	FIG 2.	5,7
	Ry		0.320	0.350	0.380	-		
	Gx		0.349	0.379	0.409	-		
	Gy		0.528	0.558	0.588	-		
	Bx		0.116	0.146	0.176	-		
	By		0.107	0.137	0.167	-		
	Wx		0.295	0.325	0.355	-		
	Wy		0.324	0.354	0.384	-		

Note 1. Contrast Ratio (CR) is defined mathematically as below, for more information see Figure 2.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 2.

Lv = Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)

Note 3. The uniformity in surface luminance δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the minimum luminance of 5 points luminance by maximum luminance of 5 points luminance. For more information see Figure 2.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

Note 4. Response time is the time required for the display to transition from white to black (Rise Time, Tr) and from black to white (Decay Time, Tf). For additional information see Figure 1. The test equipment is BM-7A.

Note 5. CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then make average value.

Note 6. For TFT module, viewing angle is the angle at which the contrast ratio is greater 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to LCD surface. For more information see Figure 3.

Note 7. Viewing angle is measured at the center point of the LCD by CONOSCOPE (ergo-80). For response time testing, the testing data is based on BM-7A. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, Chromaticity the test data is based on SR-3A.

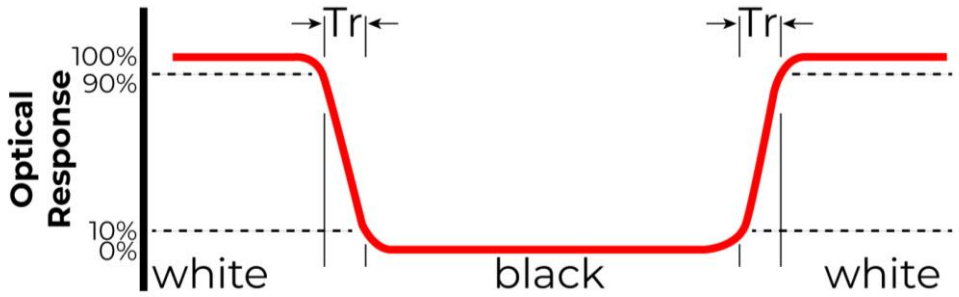
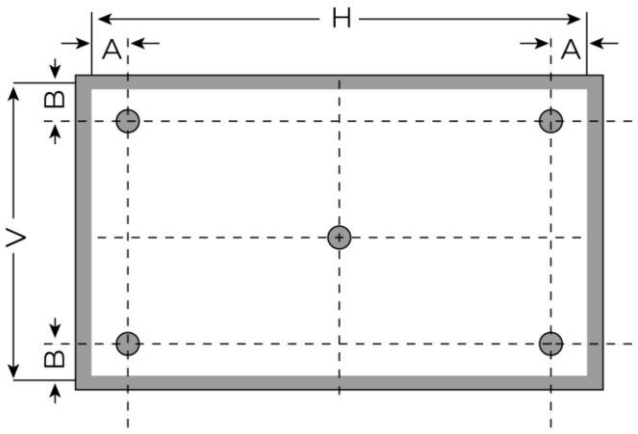


Figure 1. The definition of response time



A: 5mm

B: 5mm

H, V: Active Area

Light spot size ∅=5mm, 500mm distance from the LCD surface to detector lens.

Measurement instrument is SR-3A

Figure 2. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity

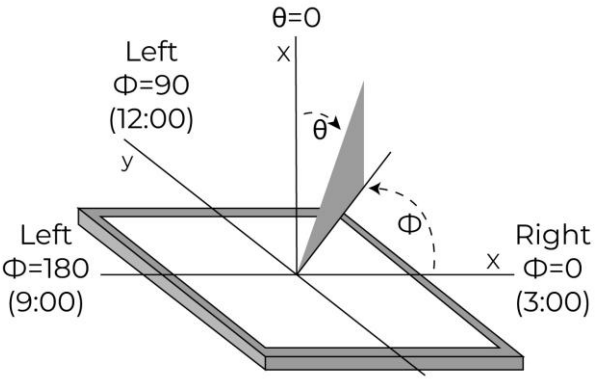


Figure 3. The definition of viewing angle

9. INTERFACES DESCRIPTION

9.1 P1 connector - RiBUS description

PIN	SYMBOL	DESCRIPTION
1	VDD	Supply voltage for module; TYP 3.3 V
2	GND	Ground
3	SPI_SCLK	SPI SCK signal
4	MISO/ IO.1	SPI MISO signal / SPI Quad mode: SPI data line 1
5	MOSI/ IO.0	SPI MOSI signal / SPI Quad mode: SPI data line 0
6	CS	SPI chip select signal
7	INT	Interrupt signal from device to the system, Active Low, internally 47k Pull UP
8	RST/PD	Reset / Power down signal, Active Low, Internally Pulled UP 47k
9	GPIO.0	GPIO.0
10	DISP_AUDIO	Display audio in/out
11	GPIO.1/IO.2	SPI Single/Dual mode: General purpose IO0. QSPI mode: SPI data line 2
12	GPIO.2/IO.3	SPI Single/Dual mode: General purpose IO1. QSPI mode: SPI data line 3
13-16	NC	Not connected
17-18	BLVDD	Supply voltage for backlight
19-20	BLGND	Backlight Ground, internally connected to GND

9.2 P2 connector description- Audio interface description

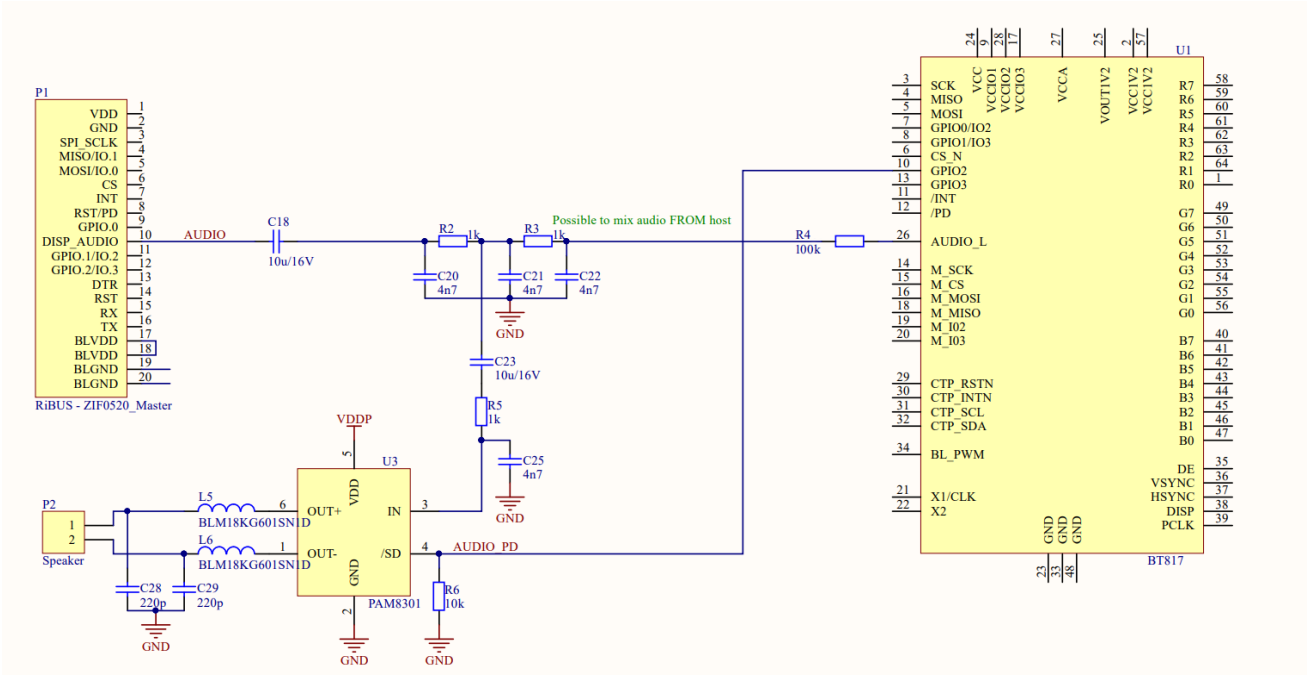
PIN NO.	SYMBOL	DESCRIPTION	NOTE
1	SPEAKER +	Speaker coil “+” terminal	Note 1
2	SPEAKER -	Speaker coil “-” terminal	

The audio circuit allows for the following 3 modes:

1. To play sounds from BT817Q on internal amplifier U3.
2. To play sounds from host on internal amplifier U3.
3. To play sounds from BT817Q on external amplifier.

Note 1. Matched Riverdi louder speaker for all EVE4 series displays: RVA-SPK1.5W-C150

Figure 5. The simplified audio circuit design



10. BT817Q CONTROLLER SPECIFICATION

BT817Q or EVE4 (Embedded Video Engine 4) simplifies the system architecture for advanced human machine interfaces (HMIs) by providing functionality for display, audio, and touch as well as an object-oriented architecture approach that extends from display creation to the rendering of the graphics.

10.1 Serial host interface

Figure 5.SPI single/dual interface connection

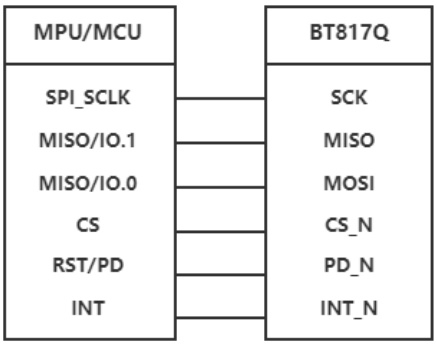
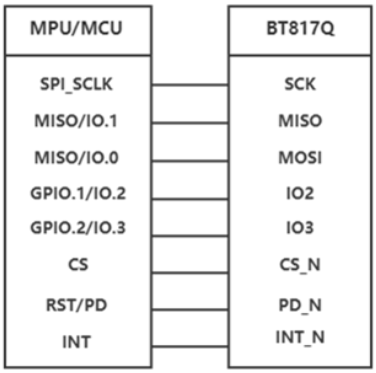


Figure 6. QSPI interface connection



SPI Interface – the SPI slave interface operates up to 30MHz.

Only SPI mode 0 is supported. The SPI interface is selected by default.

QSPI Interface – the QSPI slave interface operates up to 30MHz. Only SPI mode 0 is supported. The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.

By default, the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG_SPI_WIDTH.

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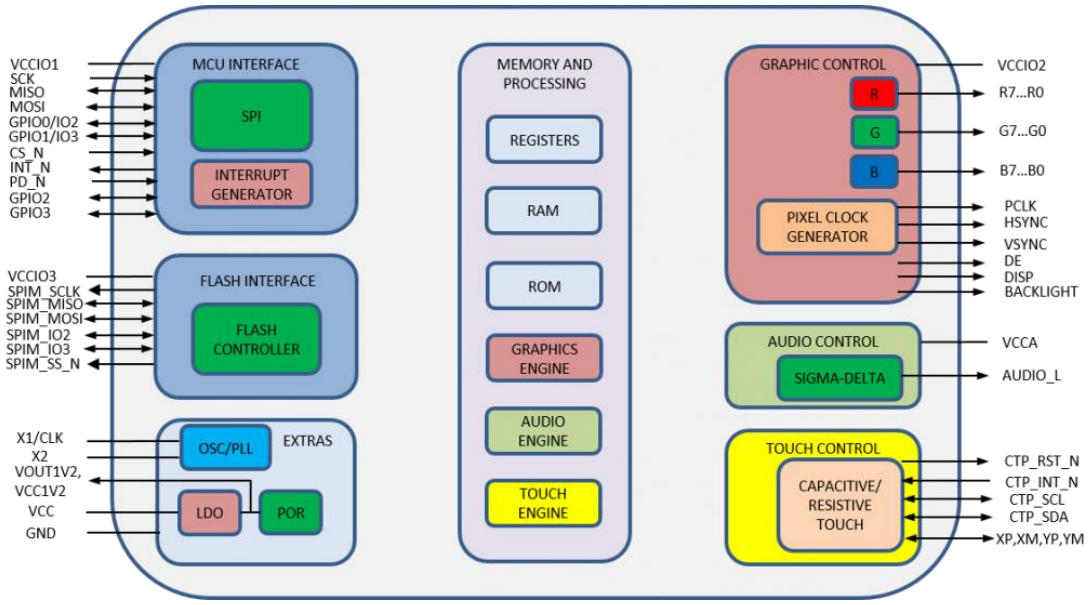
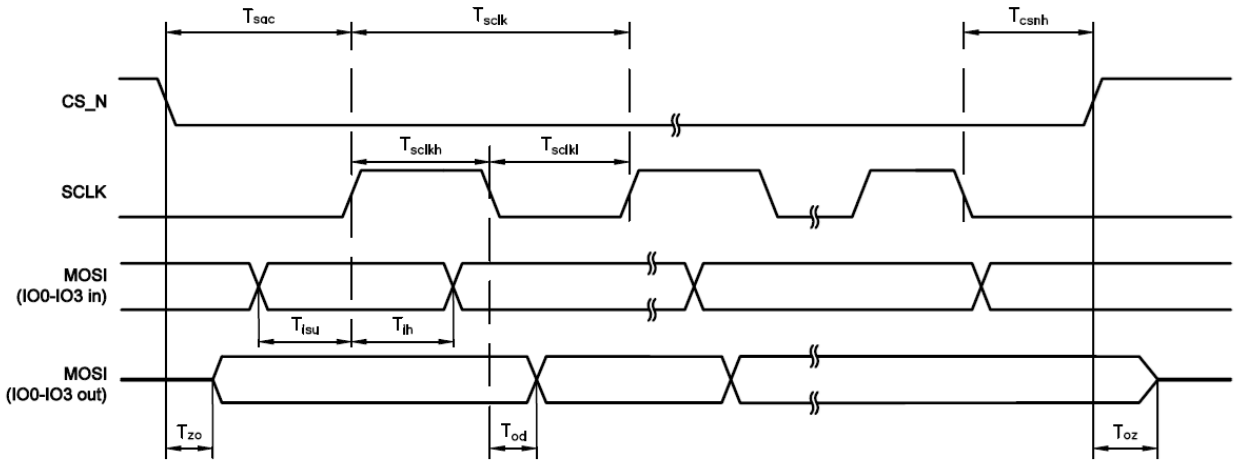
10.2 Block Diagram

Figure 7. BT817Q Block diagram



10.3 Host interface SPI mode 0

Figure 8. SPI timing diagram



PARAMETER	DESCRIPTION	VCCIO=1.8V		VCCIO=2.5V		VCCIO=3.3V		UNIT
		Min	Max	Min	Max	Min	Max	
T_{sclk}	SPI clock period	33.3	-	33.3	-	33.3	-	ns
T_{sclkl}	SPI clock low duration	13	-	13	-	13	-	
T_{sclkh}	SPI clock high duration	13	-	13	-	13	-	
T_{sac}	SPI access time	4	-	3.5	-	3	-	
T_{isu}	Input Setup	4	-	3.5	-	3	-	
T_{ih}	Input Hold	0	-	0	-	0	-	
T_{zo}	Output enable delay	-	16	-	13	11	-	
T_{oz}	Output disable delay	-	13	-	11	10		
T_{od}	Output data delay	-	15	-	12	11	-	
T_{csnh}	CSN hold time	0	-	0	-	0	-	

For more information about BT817Q controller please go to official BT81x website.

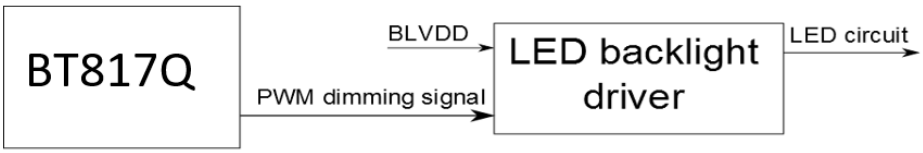
https://brtchip.com/product/bt817/

10.4 Backlight driver block diagram

Backlight enable signal is internally connected to BT817Q backlight control pin. This pin is controlled by two BT817Q's registers. **REG_PWM_HZ** specifies the PWM output frequency. The recommend PWM backlight frequency ranges from 5kHZ to 10kHZ.
REG_PWM_DUTY specifies the duty cycle.

Refer to BT817Q datasheet for more information.

Figure 9. Backlight driver block diagram



The LED backlight driver used in this module does not burst the LED current. Therefore, it does not generate audible noises on the output capacitor. It is equipped with soft start subsystem, which increases LED lifetime, as LED current peaks are reduced significantly.

11. 256MB NOR FLASH MEMORY

The Riverdi EVE4 4.3" series modules are built with a 256Mb NOR flash memory chip. Graphics assets such as fonts, audio, and images can be stored in the flash memory. Up to 270 full resolution (480 * 272 pixels, JPG) images can be stored. If you need to change the memory size, please contact: contact@riverdi.com

There is an additional port P3 for programming the flash memory directly from an external source. This port is designed to be used during production if the customer wants to order pre-programmed EVE4 boards with graphic content of their own choice.

Cable TC2050-IDC-NL is compatible with P3 programming port.

12. TFT TIMING CHARACTERISTICS

The TFT of the module applies Riverdi high brightness, IPS, 4.3” RGB TFT: RVT43HLTNWCA0

For detailed information of the display, please refer to datasheet of display.

12.1 Parallel 24-bit RGB input timing table

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	REMARK
DCLK Frequency	Fclk	8	9	12	MHz	
DCLK Period	Tclk	83	111	125	ns	
HSYNC Period Time	Th	485	531	598	DCLK	
HSYNC Display Period	Thdisp		480		DCLK	
HSYNC Back Porch	Thbp	3	43	43	DCLK	By H_blanking setting
HSYNC Front Porch	Thfp	2	8	75	DCLK	
HSYNC Pulse Width	Thw	2	4	43	DCLK	
VSYNC Period Time	Tv	276	292	321	HSYNC	
VSYNC Display Period	Tvdisp		272		HSYNC	
VSYNC Back Porch	Tvbp	2	12	12	HSYNC	By V_blanking setting
VSYNC Front Porch	Tvfp	2	8	37	HSYNC	
VSYNC Pulse Width	Tvw	2	4	12	HSYNC	

13. MODULE INITIALIZATION

Initialization data, timings and example codes are available on the Riverdi GitHub, at address: https://github.com/riverdi/riverdi-eve

REGISTER NAME	REGISTER VALUE (DEC.)
REG_HSIZE	480
REG_VSIZE	272
REG_HCYCLE	531
REG_HOFFSET	43
REG_HSYNC0	0
REG_HSYNC1	4
REG_VCYCLE	292
REG_VOFFSET	12
REG_VSYNC0	0
REG_VSYNC1	4
REG_PCLK	1
REG_SWIZZLE	0
REG_PCLK_POL	1
REG_CSPREAD	0
REG_DITHER	0
REG_PCLK_FREQ	50 (0x32)
REG_PCLK_2X	0

14. INSPECTION

Standard acceptance/rejection criteria for TFT module according to document available here.

15. RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	NOTE
1	High Temperature Storage	80°C/120 hours	A,B,C,D,E
2	Low Temperature Storage	-30°C/120 hours	
3	High Temperature Operating	70 °C /120 hours	
4	Low Temperature Operating	-20°C/120 hours	
5	High Temperature and High Humidity	+60℃, 90%RH, 120hrs	
6	Thermal Cycling Test (No operation)	-20℃/30 min ~ +70℃/30 min for a total 5 cycles, Start with cold temperature and end with high temperature.	A,B,C,D,E
7	Vibration Test	Sweep:10Hz~55Hz~10Hz 2G 2 hours for each direction of X. Y. Z. (6 hours for total)	A,B,C,D,E
8	Package Vibration Test	Random Vibration : 0.015G*G/Hz from 5-200HZ, -6dB/Octave from 200-500HZ 2 hours for each direction of X. Y. Z. (6 hours for total)	A,B,C,D,E
8	Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	A,B,C,D,E
9	ESD	Contact=+/-4KV, Air=+/-8KV,(R=330R,C=150pF), 1 sec,9point,10times/point;	A,B,C,D,E

Notes

A. LCM each function is OK.
B. LCM appearance inspection without abnormalities (Including scratch, damage, corrosion and serious deformation)
C. LCM brightness above the Min. value of Spec.
D. Luminance uniformity above the Min. value of Spec.
E. Color chromaticity within tolerance range.

16. LEGAL INFORMATION

CE marking is usually obligatory only for a complete end product. Riverdi display modules are semi-finished goods which are used as inputs to become part of the finished products.

Therefore, Riverdi display modules are not CE marked.

This is not a standalone product. It was designed as an electronic component. It needs integration with a whole system to be fully functional.

Riverdi grants the guarantee for the proper operation of the goods for a period of 12 months from the date of possession of the goods. If in a consequence of this guaranteed execution the customer has received the defects-free item as replacement for the defective item, the effectiveness period of this guarantee shall start anew from the moment the customer receives the defects-free item.

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17. CONTACT

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Stuck on a technical challenge? Need expert guidance?
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